UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,387	11/16/2001	Jeffrey Raynor	00ED18852609	4936

27975 7590 11/15/2006

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
DANIELS, ANTHONY J	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,387	RAYNOR ET AL.	
	Examiner	Art Unit	
	Anthony J. Daniels	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,13-30 and 32-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,13-30 and 32-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment, filed 9/1/2006, has been entered and made of record. Claims 11,13-30 and 32-40 are pending in the application.

Response to Arguments

2. Applicant's arguments with respect to the independent claims and claim 11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. Claims 11,13-16,18,19,21-25,27,28,30,32-36,38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) (09/993,387) in view of Lee et al. (US # 6,466,265).

As to claim **11**, AAPA teaches a solid state imaging device (Figure 5, Sophisticated Linear Array) comprising: a two-dimensional array of pixels defining an image plane (Figure 5, Image Array); and readout electronics laterally adjacent the image plane for reading signals therefrom (Figure 5, Readout Electronics); and a multiconductor signal bus connected between said array of pixels and said readout electronics (Figure 5, connection between Image Array and Readout Electronics), said multiconductor signal bus comprising a respective conductor to provide a dedicated readout channel for only one pixel of said two-dimensional array of pixels defining the image plane (Figure 5). The claim differs from AAPA in that it further requires that the readout electronics comprises at least one store circuit.

In the same field of endeavor, Lee et al. teaches a CMOS active pixel array connected to readout electronics (Figure 2A) wherein the readout electronics comprises a store circuit. In each store circuit, there exist two processing circuits and output channels (Figure 4, CDS # 1, difference amplifier # 1 and CDS # 2, difference amplifier # 2). Each of the processing circuits has a CDS (correlated double sampling) circuit (Figure 4, CDS "91") and a difference amplifier (Figure 4, difference amplifier "92"). The CDS circuitry includes two capacitors (Figure 5, "Cr" and "Cs"), one to store the sample of the reset signal and one to store a sample of the image signal (Col. 5, Lines 41-43). The difference amplifier outputs the difference of the two signals. In light of the teaching of Lee et al. it would have been obvious to one of ordinary skill in the art to include the CDS circuitry and difference amplifier of Lee et al. in the readout electronics in Figure 5 of AAPA, because an artisan of ordinary skill in the art would recognize that this would decrease the amount of fixed pattern noise in the image array.

As to claim **13**, AAPA, as modified by Lee et al., teaches a solid state imaging device according to claim 11. The claim differs from AAPA, as modified by Lee et al., in that it further requires that each pixel comprises: a photosensitive diode; and a switching circuit for resetting and discharging said diode, said switching circuit consisting of a first transistor for applying a reset pulse, and second transistor for connecting said diode to a conductor within said multiconductor signal bus.

In the same field of endeavor, Lee et al. teaches a CMOS active pixel array (Figure 2) where in each pixel comprises: a photosensitive diode (*A photosensitive diode is inherent in the CMOS pixel array of Figure 2a.*); and a switching circuit for resetting and discharging said diode (Figure 5, Cr (reset value); *{The CDS circuitry of the processing circuits "11" – "14" requires*

the reset signal of the pixel.}), said switching circuit consisting of a first transistor for applying a reset pulse, and second transistor for connecting said diode to a conductor (Col. 1, Lines 59-61, "...active pixel sensors...") within said multiconductor signal bus (Figure 2a). In light of the teaching of Lee et al., it would have been obvious to one of ordinary skill in the art to make the image array of Raynor a CMOS active pixel array, because an artisan of ordinary skill in the art would recognize that this would allow for lower power consumption and the ability to implement other circuits and the array on a single chip.

As to claim **14**, AAPA, as modified by Lee et al. teaches a solid state imaging device according to Claim 11, wherein said multiconductor signal bus comprises plurality of vertically stacked conductors (see AAPA, Figure 5).

As to claim **15**, AAPA, as modified by Lee et al. teaches a solid state-imaging device according to Claim 11, wherein said readout electronics are laterally adjacent one side of the image plane (see AAPA, Figure 5).

As to claim **16**, AAPA, as modified by Lee et al. teaches a solid state imaging device according to Claim 11, wherein said readout electronics are laterally adjacent two opposing sides the image plane (see AAPA, Figure 5).

As to claim **18**, AAPA, as modified by Lee et al., teaches a solid state imaging device according to Claim 11, wherein said at least one store circuit comprises plurality of store circuits (see Lee et al., CDS # 1-N) with a store circuit corresponding to each pixel (see Lee et al., Col. 5, Lines 38-42) and comprising: a first storė circuit for storing a first reset value (see Lee et al., Figure 5, capacitor "Cr"; Col. 5, Lines 36-43); and a second store circuit for storing a read out value (see Lee et al., Figure 5, capacitor "Cs"; Col. 5, Lines 36-43), with the read out value of a

given pixel being modified by the stored reset value that pixel (see Lee et al., Col. 5, Lines 43-46; *{The difference amplifier "93" of Figure 5 subtracts the reset value from the signal value.}*).

As to claim **19**, AAPA, as modified by Lee et al., teaches a solid state imaging device according to Claim 18, wherein each store circuit further comprises: a third store circuit for storing a second reset value (Figure 2a, Figure 5, capacitor "Cr" of CDS # 2 and difference amplifier # 2), with a current reset value (Figure 2a, Figure 5, reset value on capacitor "Cr" of CDS # 1) and a current read out value (Figure 2a, Figure 5, signal value on capacitor "Cs" of CDS # 1) being processed simultaneously based upon application a new reset pulse (Col. 1, Lines 59-67; Col. 2, Lines 1-8).

As to claim **21**, the limitations of claim 21 can be found in claims 11 and 13. Therefore claim 21 is analyzed and rejected as previously discussed with respect to claims 11 and 13.

As to claim **22**, AAPA, as modified by Lee et al., teaches a solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus (see AAPA, Figure 5); and wherein said switching circuit consisting of a first transistor for applying a reset pulse, and second transistor for connecting said diode to a conductor (see Lee et al., Col. 1, Lines 59-61, "...active pixel sensors...") within said multiconductor signal bus (see Lee et al., Figure 2a).

As to claim **23-25,27** and **28**, the limitations in claims 23-25,27 and 28 can be found in claims 14-16,18 and 19, respectively. Therefore, claims 23-25,27 and 28 are analyzed and rejected as previously discussed with respect to claims 14-16,18 and 19, respectively.

As to claims **30,34-36,38** and **39**, claims 30,34-36,38 and 39 are method claims corresponding to the apparatus claims 11,14-16,18 and 19, respectively. Therefore, claims 30,34-

36,38 and 39 are analyzed and rejected as previously discussed with respect to the apparatus claims 11,14-16,18 and 19, respectively.

As to claim **32**, AAPA, as modified by Lee et al. teaches a method according to Claim 30, further comprising forming each pixel to have a photosensitive diode (*A photosensitive diode is inherent in the CMOS pixel array of Figure 2a of Lee et al.*), and a switching circuit connected thereto for resetting and discharging the diode (see Lee et al., Figure 5, Cr (reset value); *{The CDS circuitry of the processing circuits "11" – "14" requires the reset signal of the pixel.}*).

As to claim **33**, AAPA, as modified by Lee et al., teaches a method according to Claim 32, wherein the switching circuit consists essentially of a first transistor for applying a reset pulse, and second transistor for connecting said diode to a conductor (see Lee et al., Col. 1, Lines 59-61, "...active pixel sensors...") within said multiconductor signal bus (see AAPA,Figure 5).

4. Claims 17,26 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (09/993,387) in view of Lee et al. (US # 6,466,265) in view of Fossum (US # 6,667,768) and further in view of Miyazaki et al. (US # 6,130,712).

As to claim **17**, AAPA, as modified by Lee, teaches a solid state-imaging device according to Claim 11. The claim differs from AAPA, as modified by Lee et al., in that it further requires that all pixels of said array of pixels are reset simultaneously and are read out simultaneously.

In the same field of endeavor, Fossum teaches a CMOS active pixel array utilizing a global shutter effect, wherein the all pixels of the array are reset simultaneously (Col. 1, Lines 23 and 24). In light of the teaching of Fossum, it would have been obvious to one of ordinary skill

in the art to reset the pixels of the array of AAPA simultaneously, because an artisan of ordinary skill in the art would recognize that this would freeze moving objects, thereby eliminating motion blur (see Fossum et al., Col. 1, Lines 24 and 25).

In the same field of endeavor, Miyazaki et al. teaches a linear pixel array (Figure 1) wherein the charges from the pixels are readout simultaneously (Col. 3, Lines 33-40). In light of the teaching of Miyazaki et al., it would have been obvious to one of ordinary skill to readout the charges from the pixels of AAPA, because an artisan of ordinary skill in the art would recognize that this would allow for quicker transmission and ensure a uniform exposure period.

As to claim **26**, the limitations of claim 26 can be found in claim 20. Therefore, claim 29 is analyzed and rejected as previously discussed with respect to claim 20.

As to claim **37**, claim 37 is a method claim corresponding to the apparatus claim 17. Therefore, claim 37 is analyzed and rejected as previously discussed with respect to claim 17.

5. Claims 20,29,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (09/993,387) in view of Lee et al. (US # 6,466,265) and further in view of in view of Decker et al. (US 20020154231).

As to claim **20**, Lee et al. teaches a solid state imaging device according to Claim 19, wherein said readout electronics further comprises: a differential amplifier (Figure 5, difference amplifier "93") connected to said first, second and third store circuits (Figure 2a, Figure 2e, Figure 5). The claim differs from Lee et al. in that it further requires a reset circuit for placing said differential amplifier a common mode reset state prior to reading a signal.

In the same field of endeavor, Decker et al. teaches a CMOS imaging array (Figure 3) with readout electronics including a CDS circuit including a difference amplifier (Figure 7, amp "700") that is put into a common-mode state upon receiving a pulse signal at a transistor (Figure 7, transistor "M705"; ϕ1; [0065], Lines 7-15). In light of the teaching of Decker et al., it would have been obvious to one of ordinary skill in the art to include the ability of the difference amplifier of Lee et al. to be put in a common-mode state thereby ensuring the correct difference between the signal values and reset values.

As to claim **29**, the limitations of claim 29 can be found in claim 20. Therefore, claim 29 is analyzed and rejected as previously discussed with respect to claim 20.

As to claim **40**, claim 40 is a method claim corresponding to the apparatus claim 20. Therefore, claim 40 is analyzed and rejected as previously discussed with respect to claim 20.

Conclusion

6. *The examiner feels that line arrays and particularly the two-dimensional (two rows) one of Figure 5, with a slight modification of Lee, still reads on the claim. However, in Table 1 of Page 10 of the specification, the pixel array is 100 x 100. An amendment of this sort would overcome the line sensors exemplified in Figure 5. Also, linear arrays in the prior art come with 3 rows, one for each color (i.e. RGB). Amending the claim to state the array contains more than 2 rows would overcome the line array of Figure 5, but not the aforementioned 3 row linear arrays in the prior art. These arrays have not been made of record in this case.*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD
11/7/2006

NGOC YEN VU
SUPERVISORY PATENT EXAMINER